FUSED BOOTH ENCODER MULTIPLEXER

ABSTRACT OF THE DISCLOSURE

A multiplier circuit comprises a fused Booth encoder multiplexer which produces partial product bits, a tree which uses the partial product bits to generate partial products, and an adder which uses the partial products to generate intermediate sum and carry results for a multiplication operation. The fused Booth encoder multiplexer utilizes encoder-selector cells having a logic tree which carries out a Boolean function according to a Booth encoding and selection algorithm to produce one of the partial product bits at a dynamic node, and a latch connected to the dynamic node which maintains the value at an output node. The encoder-selector cells operate in parallel to produce the partial product bits generally simultaneously. A given one of the encoder-selector cells has a unique set of both multiplier operand inputs and multiplicand operand inputs, and produces a single partial product bit. The fused Booth encoder multiplexer unit, tree unit and adder unit function in a pipeline manner with the units operating on sequential data sets during a given processing cycle. The fused Booth encoder multiplexer unit may be advantageously laid out in a design of an integrated circuit chip with no gap present in the layout, which allows uniform wire length and avoids the necessity of large transistors to drive long interconnection wires.